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Title of the Invention

SEMICONDUCTOR MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME

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DESCRIPTION

SEMICONDUCTOR MEMORY DEVICE AND METHOD OF

MANUFACTURING THE SAME

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TECHNICAL FIELD

The present invention relates to a semiconductor memory device, such as a dynamic random access memory having a capacitor of a three-dimensional structure
10 suitable for high density device integration or to a static random access memory, and also to an embedded memory system LSI using those memory elements as cores.

BACKGROUND ART

15 For example, the dynamic random access memory (hereafter referred to as a dynamic RAM) has as an elemental memory unit a memory cell having connected thereto a capacitor to store electric charge as one bit of information and a switch transistor to write or read information
20 into or from the capacitor. As it forms one memory cell by the small number of component elements as described above, the dynamic RAM is widely used in the main memory of computer equipment that requires a large capacity.

To increase the memory capacity of the dynamic
25 RAM, it is necessary to miniaturize the memory cell area to increase the density of the memory cells.

However, in such a process, by the reduction of the memory cell area, the effective area of the charge-

storage capacitor of the memory cell is decreased and the storage capacitance decreases. Therefore, the so-called soft-error phenomenon has manifested itself that information in the memory cell is reversed by a decrease

5 of S/N ratio or by alpha-ray exposure, and has become a serious problem of reliability.

For this reason, there have been devised several memory cell structures that provide a large storage capacitance without increasing the area occupied by the

10 memory cell. One of them is a memory cell having a stacked capacitor formed as a three-dimensional capacitor that uses the vertical material faces of the storage capacitance electrode as in the crown-shaped capacitor. Memory cells of this kind are described in JP-A-62-48062

15 and JP-A-62-128168, for example.

The memory cell of a 1-gigabit dynamic RAM is discussed in IEEE Int., Electron Devices Meeting, Technical Digest, pp.927-929 Dec. (1994).

The dynamic RAM that the present inventors have

20 conceived based on the memory cell structure disclosed in the above-mentioned literature is shown in Fig. 45. The structure and problem of this dynamic RAM will be described with reference to Fig. 45.

In Fig. 45, a transistor as a switch for the

25 memory cell (hereafter a MISFET, which is in most general use, is used) includes a gate insulator 403, a gate electrode 404 and highly-doped n-type impurity regions 407, 408 as the source or the drain. In the highly-doped n-type

impurity regions 407, 408, there are polycrystalline-silicon plugs 410 that pierce through a silicon dioxide film 409. There is an opening through a insulating film 412 on the polysilicon plug 410. Through this polysilicon

5   plug, a data line (wiring electrode 413) formed on the insulating film 412 is electrically connected to the highly-doped n-type impurity region 407. In a space between the data line (wiring electrode 413) and a word lines (gate electrodes 404), there is formed a common

10   opening, which runs through the insulating film 412 on the polysilicon plug 410 in the highly-doped n-type impurity region 408 and a silicon dioxide film 414 on the insulating film 412. Through this opening and the polysilicon plug 410, a storage electrode 415 of a crown-

15   shaped capacitor formed of the above-mentioned polysilicon is electrically connected to the highly-doped n-type impurity region 408.

       A capacitor dielectric film 416 is deposited on the storage electrode 415, and a plate electrode 417 is

20   provided on the capacitor dielectric film 416. An aluminum wiring 419, formed on the silicon dioxide film 418 on the memory cell, is used as the cell selection wire or the main word line.

       However, in a memory cell that has a capacitor

25   above the data line as mentioned above, particularly, in the same memory cell when it is used for high device integration, the connection point of the data line (wiring electrode 413) and that of the capacitor electrode 415 are

inevitably arranged very close to each other. Therefore, it becomes difficult to secure sufficient electrical insulation between the data line and the capacitor electrode due to mask misalignment during manufacture or a

5 shift in dimensions (side etching) in dry etching in forming the opening of the insulating film 414. There is another problem. In matching of the data line to the opening of the insulating film 412, it becomes difficult to secure a sufficient allowance of the data line to

10 overlie the opening. Owing to mask misalignment or a dimensional shift (side etching) in the dry etching of the wiring electrode 413 as the data line, there os a possibility that the polysilicon plug 410 is exposed from the above-mentioned opening and etched deeper.

15   Further, it has been necessary to arrange peripheral circuits, such as sense amplifiers, which are directly connected to the memory cell array, at the same pitch as the memory cells or at a twice larger pitch. In a memory for high device integration, which has a small area,

20 it has been necessary to reduce the area occupied by the direct peripheral circuits, such as the sense amplifiers. Also in the indirect peripheral circuit, there are the same problems as with the memory cell as mentioned above in reducing the area occupied by the MISFET as a component

25 part of the indirect peripheral circuit and in improving the wiring density.

        Further, because a three-dimensional capacitor with a considerable height is used for the memory cell, if

such a height difference between the memory cell portion and the indirect peripheral circuit portion is smoothed out, a problem has arisen that the depth of the contact holes in the indirect peripheral circuit portion increases

5   and disconnection occurs in the indirect peripheral circuit.

To solve this problem, it is effective to use polysilicon plugs the same as used for the memory cells also for the contact areas of the indirect peripheral

10 circuit. Doped polysilicon has conventionally been used to form polysilicon plugs, and therefore polysilicon plugs of doped polysilicon could be used for memory cells comprising transistors of one conductivity type.

However, in the indirect peripheral circuit

15 where transistors of different conductivity types are generally used, polysilicon plugs of doped polysilicon of one conductivity type could not be used and therefore it has been difficult to reduce the areas of the indirect peripheral circuits.

20   On the other hand, as a plug material such as mentioned above, tungsten is well known which is deposited by chemical vapour deposition (CVD). In this case, tungsten can be used for the indirect peripheral circuit because tungsten serves as the diffusion barrier against

25 impurities, but a problem has presented itself that tungsten has a low heat resistance and reacts with silicon during heat treatment at 600°C or higher.

Also in a static random access memory (hereafter

referred to simply as a static RAM) cell made of transistors of opposite conductivity types formed on the principal surface of the silicon substrate, the memory cell area could be reduced by local interconnect

5   technology. But, with technologies of this kind, it has not become possible to install the wiring layers of the indirect peripheral circuit.

Further, in an embedded memory system LSI (semiconductor integrated circuit system) using high-

10   density dynamic, it is essential to use as many parts common to the memory cell and logic regions as possible.

DISCLOSURE OF THE INVENTION

An object of the present invention is to provide

15   a semiconductor memory device, which includes a memory cell and indirect peripheral circuit and which has high component integration and high reliability.

Another object of the present invention is to provide a semiconductor memory device, which includes a

20   memory cell and complementary transistors that form a sense amplifier or a logic circuit, and which has high component integration and high reliability.

Yet another object of the present invention is to provide a dynamic RAM having stacked capacitors in high

25   density and with increased storage capacity.

A still further object of the present invention is to provide a dynamic RAM with a reduced memory cell area.

The present invention has been made to provide a semiconductor memory device which enables cost reduction by simplifying the manufacturing process.

According to the present invention, a
5 semiconductor memory device having a memory cell and its indirect peripheral circuit, comprising:

transistors provided on a principal surface of a semiconductor surface;

a first insulating film provided on the
10 transistors;

a plurality of first conductors (plug electrodes) passing through the first insulating film and being made of titanium nitride having superior covering properties; and

15 a first wiring provided on the principal surface of the first insulating film,

wherein the first wiring is connected to the transistors by the first conductors.

According to the present invention, in a memory
20 cell region, a capacitor and a transistor formed on a principal surface of a second insulating film on the first insulating film are connected by the second conductor that pass through the first conductor and the second insulating film.

25 According to the present invention, the second conductor is formed so that its cylindrical portion is smaller than the diameter of the cylindrical portion of the first conductor.

Further according to the present invention, the first wiring is formed so that its line width is thinner than the diameter of the cylindrical portion of the first conductor.

5   Still further according to the present invention, a n-channel transistor and a p-channel transistor, which constitute a complementary transistor, are electrically connected by the first conductor.

According to the present invention, the first
10   conductor made of titanium nitride effectively functions as the etching stopper to dry etching of the first wiring by using a suitable material for the first wiring and thus effectively utilizing a difference in etching rate between the first conductor and the first wiring.

15   Therefore, even if the first wiring connected to the first conductor is arranged in such a way that the first wiring does not completely cover the first conductor exposed at the principal surface of the first insulating film, the first conductor is prevented from being etched
20   deeper when the first wiring is dry etched.

Because the diameter of the cylindrical portion of the second conductor and the line width of the first wiring are both thin, a contact does not occur between the second conductor and the first wiring.

25   Therefore, even if the area for the memory cell is reduced, a short-circuit never occurs between the capacitor and the data line, and because the capacitor is located above the data line, the required area for the

capacitor in the memory cell can be increased to a maximum.

Further, because the titanium nitride serves as the barrier to diffusion of impurities, the first conductor is used to connect the n-channel transistor and

5   the p-channel transistor in indirect peripheral circuit devices or in a static RAM cell formed by complementary transistors, so that the required areas for the indirect peripheral circuit and a memory cell can be reduced.

10   BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sectional view of a semiconductor memory device according to a first embodiment of the present invention;

Fig. 2 is a plan view of the semiconductor

15   memory device according to the first embodiment of the present invention;

Fig. 3 is an equivalent circuit diagram of the semiconductor memory device according to the first embodiment of the present invention;

20   Figs.4 to 10 are sectional views for explaining the manufacturing process of the semiconductor memory device according to the first embodiment of the present invention;

Fig. 11 is a sectional view of the semiconductor

25   memory device according to a second embodiment of the present invention;

Fig. 12 is a sectional view of the semiconductor memory device according to the second embodiment of the

present invention;

Fig. 13 is a sectional view of the semiconductor memory device according to a third embodiment of the present invention;

5   Figs.14 to 17 are sectional views for explaining the manufacturing process of the semiconductor memory device according to the third embodiment of the present invention;

Fig. 18 is a sectional view of the semiconductor

10   memory device according to a fourth embodiment of the present invention;

Figs.19 to 24 are sectional views for explaining the manufacturing process of the semiconductor memory device according to the fourth embodiment of the present

15   invention;

Fig. 25 is a sectional view of the semiconductor memory device according to a fifth embodiment of the present invention;

Figs.26 to 31 are sectional views for explaining

20   the manufacturing process of the semiconductor memory device according to the fifth embodiment of the present invention;

Fig. 32 is an equivalent circuit diagram of the semiconductor memory device according to a sixth

25   embodiment of the present invention;

Fig. 33 is a plan view of the semiconductor memory device according to the sixth embodiment of the present invention;

Fig. 34 is a plan view of the semiconductor memory device according to the sixth embodiment of the present invention;

Fig. 35 is a sectional view of the semiconductor memory device according to the sixth embodiment of the present invention;

Fig. 36 is a plan view of the semiconductor memory device according to a seventh embodiment of the present invention;

Fig. 37 is a plan view of the semiconductor memory device according to the seventh embodiment of the present invention;

Fig. 38 is a sectional view of the semiconductor memory device according to the seventh embodiment of the present invention;

Fig. 39 is a plan view of the semiconductor memory device according to an eighth embodiment of the present invention;

Fig. 40 is a sectional view of the semiconductor memory device according to the eighth embodiment of the present invention;

Fig. 41 is a plan view of the semiconductor memory device according to a ninth embodiment of the present invention;

Fig. 42 is a plan view of the semiconductor memory device according to the ninth embodiment of the present invention;

Fig. 43 is a sectional view of the semiconductor

memory device based on the idea of the present invention prior to the present invention;

Fig. 44 is a sectional view of the semiconductor memory device according to the first embodiment of the present invention; and

Fig. 45 is a sectional view of the semiconductor memory device according to the first embodiment of the present invention.

BEST MODE OF CARRYING OUT THE INVENTION

The present invention will be described in detail with reference to preferred embodiments.

<Embodiment 1>

Referring to Figs.1 to 10, description will be made of an embodiment of a dynamic RAM according to the present invention. Fig. 1 shows a sectional view of the memory cell and a sectional view of the MISFET portion of the indirect peripheral circuit depicted together the same drawing. Fig. 2 is a plan view of the memory cell. The sectional view of the memory cell portion in Fig. 1 corresponds to a part of the cross section taken along the line X-X' in Fig. 2.

In Fig. 1, a MISFET in the memory cell consists of a gate insulating film 3, a gate electrode 4, and highly-doped n-type impurity regions 7, 8 as the source and drain. A MISFET in the indirect peripheral circuit consists of a gate insulating film 3, highly-doped p-type impurity regions 9 as the source and drain. Generally, a

complementary MISFET (a CMISFET or more specifically a CMOSFET) is used in the indirect peripheral circuit. In the present invention, too, description presupposes the use of n-channel and p-channel transistors as the indirect

5   peripheral circuit elements. However, description is limited to the p-channel transistor.

Plug electrodes 11 made of titanium nitride are used both in the highly-doped n-type impurity regions 7, 8 and in the highly-doped p-type impurity regions 9. The

10   plug electrode on the highly-doped n-type impurity region 7 of the memory cell is connected to a wiring electrode 13 as the data line. A storage electrode (bottom electrode) 15 of a crown-shaped capacitor is provided above the data line 13. The storage electrode 15 is connected to the plug

15   electrode 11 on the highly-doped n-type impurity region 8, and is electrically connected to the MISFET. In the silicon dioxide film 14 as the inter-layer dielectric, there is formed an opening that is smaller than in diameter than the plug electrode 11, and the storage

20   electrode 15 is connected to the plug electrode 11 through this opening. A capacitor dielectric film 16 is deposited on the storage electrode 15, and a plate electrode 17 of the capacitor is provided on top of the capacitor dielectric film 16, thus forming the crown-shaped

25   capacitor.

On the other hand, the plug electrodes 11 are formed on the highly-doped p-type impurity regions 9 as the source and drain of the MISFET and also on the gate

electrode 4. As shown in Fig. 1, common plug electrodes 11 can be provided similarly for the gate electrode 4 and the highly-doped p-type impurity region 9. As mentioned

5 earlier, the MISFET may be of the n-channel type or of the p-channel type, and the gate electrode may be of n-type or p-type conductivity. Moreover, the wiring electrode 13 may be connected to the plug electrodes of the indirect peripheral circuit to use as wiring of the indirect peripheral circuit.

10 Referring to the plan view of the memory cell in Fig. 2, the planar positional relationship of the MISFET and the capacitor in the memory cell will be described. In Fig. 2, the word line 21 is formed by a common gate electrode 4 (Fig. 1) of the MISFETs, and the data line 23

15 is formed by the wiring electrode 13 (Fig. 1). The word lines are laid in the Y-direction and the data lines are laid in the X-direction, and the crown-shaped capacitors 25 (storage electrodes 15) are formed above the word lines and the data lines. The capacitor 25 is connected through

20 an opening 24 to the plug electrode 11 in the active region (T-region) in the space between the word line and the data line. It is not necessary to provide the data line 23 with an overlay margin with respect to the opening 22. Therefore, the data line 23 is made in a so-called

25 dog-bone free structure as shown in Fig. 2.

The above-mentioned dog-bone free structure can be applied in exactly the same way to the indirect peripheral circuit. For example, Fig. 3 shows a latch-type

sense amplifier, but the present invention as shown in Fig.
1 can be effectively applied to a flip-flop circuit, such
as is formed by having a pair of CMISFETs as inverters in
the sense amplifier arranged (Lin cross connection. The

5   above-mentioned sense amplifier in Fig. 1 shows the
repetition unit, and the data pair lines connected to the
adjacent memory cell are divided into data pair lines D1
and D1B and data pair lines D2 and D2B. A data-pair-line
select line ISO1 or ISO2 separates the lines of each pair.

10 The above-mentioned flip-flop circuit is connected to the
data pair lines, and a signal sensed by the data line is
amplified by driving the common source line SNL to ground
potential and SPL to the power supply voltage. Switch
transistors connected to the I/O signal lines are further

15 connected to the data pair lines, and a row select line YL
controls input and output of a signal.

        The first embodiment of the present invention
will be described in greater detail by referring to the
sectional views of the manufacturing process in Figs.4 to

20 10. Figs. 4 to 10 show the memory cell region and the
indirect peripheral circuit region depicted together in
the same drawing as in Fig. 1.

        As shown in Fig. 4, an isolation (field oxide
film) 2 is selectively formed in a silicon substrate 1

25 having a crystal plane (100) by a well-known technique. In
the active regions demarcated by the isolation 2, MISFETs,
each having a gate electrode 4 and highly-doped n-type
impurity regions 7, 8 or highly-doped p-type impurity

regions 9, are formed by well-known methods. The gate of
the MISFETs is 0.2 μm in length. In the formation of the
isolation, various method may be used, such as a selective
oxidation method (LOCOS) or trench isolation that has a

5   silicon dioxide film entrenched in a shallow groove of a
silicon substrate. In this case, n-channel MISFETs are
used, but p-channel types may be used. Furthermore, a LDD
(Lightly Doped Drain) structure may be used to reduce the
device deterioration by hot carriers. To use self-aligned

10   contact to the gate in order to avoid a formation of gate
to contact short circuit by dry etching, silicon nitride
films 5, 6 are provided at the top or to the sidewalls of
the gate electrode 4 by a well-known method as shown in
Fig. 4.

15   Subsequently, as shown in Fig. 5, a silicon
dioxide film 10 containing boron and phosphorus is
deposited by a well-known CVD method, and the surface of
the silicon dioxide film 10 is smoothened by annealing at
a temperature of about 800°C. The silicon dioxide film may

20   be flattened by a method such as a well-known CMP
(Chemical Mechanical Polishing). Then, openings 39, 40
about 0.2 μm in diameter are formed in the silicon
dioxide film 10 by photolithography and dry etching of the
silicon dioxide film. In this step, photolithography using

25   excimer laser is carried out. In dry etching, it is
preferable to form a silicon nitride film serving as the
etching stopper at the lower portion of the silicon
dioxide film 10 and form the openings by self-alignment to

the isolation region. Preferably, the opening 40 that includes the portion where there is the gate electrode should be formed by photolithography and dry etching, which are performed separately from the similar processes

5 mentioned above. Note that when the etching stopper mentioned above is used, dry etching should be carried out both on the silicon dioxide film and the silicon nitride film.

After this, as shown in Fig. 6, a titanium

10 nitride (TiN) film is deposited to a thickness of about 300nm by a well-known CVD technique, and the titanium nitride is etched back by anisotropic dry etching, and plug electrodes (titanium nitride : TiN) 11 are formed in the above-mentioned openings 39, 40. In this case, it is

15 possible to simultaneously flatten the surface and form plug electrodes by polishing the titanium nitride film and the silicon dioxide film 10. Besides titanium nitride, a heat-resistant barrier material, such as titanium-tungsten (W) may be used.

20 Subsequently, as shown in Fig. 7, a silicon nitride film 12 with a thickness of about 50nm is deposited by a LPCV process, openings 22 (Fig. 2) are formed by photolithography and dry etching, tungsten is deposited to a thickness of about 100nm as the wiring

25 electrodes 13 and the deposited tungsten is patterned by photolithography and dry etching. Incidentally, as a material for the wiring electrodes 13, a high refractory metal other than tungsten or, for example, a composite

film of a silicide film, which is a high refractory metal, and a polysilicon film can be used.

   After this, as shown in Fig. 8, a silicon dioxide film 14 with a thickness of about 0.5 to 1 μm is

5 deposited at a temperature of about 400°C by a well-known CVD process using TEOS (tetra-ethyl-ortho-silicate) gas, and the surface is flattened by a well-known CMP method. Subsequently, openings 25 are formed in the silicon dioxide film 14 and the silicon nitride film 12. The

10 diameter of the openings is about 0.1 μm.

   As shown in Fig. 9, a first polysilicon film highly doped with n-type impurities is deposited (not shown) to a thickness of about 100nm by a well-known LPCVD method. In this case, this polysilicon film is embedded in

15 the openings 25. Though not shown, a silicon dioxide film with a thickness of about 500nm is deposited and is patterned by photolithography and dry etching to form the storage electrodes. After this, a second polysilicon film is deposited with better step coverage by LPCVD, and by

20 etching the first and second polysilicon films by anisotropic dry etching and removing the silicon dioxide film about 500nm thick mentioned above, crown-shaped storage electrodes 15 are formed. Note that before removing the silicon dioxide film mentioned above, it is

25 desirable to have a silicon nitride film provided at a bottom layer of the silicon dioxide film.

   After this, as shown in Fig. 10, a capacitor dielectric film 16, such as tantalum pentoxide (Ta_2O_5) film

is deposited, which has a greater dielectric constant than the silicon dioxide film. In this case, a CVD process for better step coverage is used as a deposition method. The effective oxide thickness of the capacitor dielectric film

5   should preferably be 3nm or less for a large-capacity dynamic RAM of 1-giga-bit class. Incidentally, here the polysilicon film is used for the storage electrodes 15, but a high refractory metal film, such as tungsten or titanium nitride, may be used. In this case, the effects

10 of the natural oxide on the surface of the polysilicon film can be avoided, and the effective oxide thickness of the capacitor dielectric film can be decreased. As the material for the capacitor dielectric film, it is possible to use well-known high ε dielectrics such as a $SrTiO_3$ film

15 and a $(Ba, Sr) TiO_3$ film (BST film) or a ferro-electric film in addition to a composite film of silicon nitride and a silicon dioxide film. After this, a high refractory metal film, such as tungsten or titanium nitride, is deposited to a thickness as large as 300nm and is

20 processed by photolithography and dry etching to form a capacitor plate electrode 17 (top electrode). As the method for depositing a material for the plate electrode, a CVD method for better step coverage should preferably be used.

25   Next, as the inter-layer insulating film, a silicon dioxide film 18 about 200nm thick is deposited, openings are formed in the silicon dioxide films 14, 18 above the metal wiring 13, and after this, a metal wiring

19 is formed, thus completing a semiconductor device according to the present invention. A low resistivity metal such as aluminum is preferred for the metal wiring 19, and and may be used for wiring inside of a memory

5   array as shown in Fig. 1. Further, a well-known plug technology or CMP method may be used to flatten the inter-layer dielectric when forming the metal wiring 21.

It ought to be noted that a greater storage capacity can be obtained by making undulated the surface

10   area of the polysilicon storage electrode 15 in the first embodiment to increase its surface area. In the first embodiment, titanium nitride is used for the plug electrodes, but titanium-tungsten (TiW) may be used, or another material that is slower in etching rate in dry

15   etching of the wiring electrode 13 and that serves as a barrier to impurity diffusion may be used.

Further, as shown in Fig. 44, if titanium (Ti) 146 is provided at the underside of the plug electrodes 11 and titanium silicide ($TiSi_2$) 147 is formed at the

20   interface the titanium and the silicon substrate, it is possible to prevent an increase in contact resistance with the highly-doped impurity regions 7, 8 and 9.

Further, as shown in Fig. 45, polysilicon plugs 248 may be placed on the highly-doped impurity regions 8

25   at the storage nodes at which the capacitors are connected. In this case, because the titanium nitride or titanium silicide does not directly contact the highly-doped impurity regions at the storage nodes, the junction

leakage current can be reduced.

According to the first embodiment, because the plug electrodes 11, which connect the data lines to the highly-doped n-type impurity regions of titanium nitride, are made of titanium nitride, even if the plug electrode lying underneath the data line is exposed during etching the data line material, the plug electrode is not etched, so that the overlay margin for openings for connection between datalines can be reduced.

Further, the storage electrode of the capacitor is not directly connected to the silicon substrate but connected through the intermediary of the plug electrode, a smaller amount of etching is required in dry etching when forming the openings for connection to the storage electrodes, and the swell at the openings due to side etching resulting from dry etching can be decreased. Consequently, the short margin between the storage electrode and the data line increases. At the plug electrode connected to the storage electrode, because the diameter of the plug electrode is smaller than the diameter of the opening, the short margin between the storage electrode and the data line further increases.

Further, because the plug electrode can be used not only on the n-channel MISFETs but also on the p-channel MISFETs in the memory cell and in the indirect peripheral circuit, the area required for indirect peripheral circuits, such as a sense amplifier, can be reduced without increasing the process steps.

Further, as described above, even if the underneath plug electrode is exposed in dry-etching the data line during dry-etching the data line material, it is not etched. Therefore, if the line width of the data lines

5   is decreased, no problem arises. Thus, the data lines and the storage electrodes are connected, the short margin of the openings can be increased. More specifically, with the wiring electrode 13 protected by photoresist in the indirect peripheral circuit region, the wiring electrode

10   13 in the memory cell region is side-etched by isotropic dry etching. Accordingly, the wiring electrode 13 in the memory cell can be decreased in thickness while the wiring electrode 13 in the indirect peripheral circuit region can be made thick at the same time. Therefore, the depth of

15   the opening for the storage electrode in the memory cell can be made shallow, so that the manufacturing process can be made easier. Incidentally, for dry etching the wiring electrode 13, by side etching the material used, the size of the dry-etching mask itself may be reduced to less than

20   the minimum-processing dimension.

<Embodiment 2>

This embodiment, which concerns the dynamic RAM in the first embodiment but uses a capacitor of a different structure from that of the first embodiment, will be described with reference to Figs. 11 and 12.

25   will be described with reference to Figs. 11 and 12.

Fig. 11 is a sectional view of the dynamic RAM according to a second embodiment. In Fig. 11, the storage electrode 26 (lower electrode) of the capacitor is formed

by a thick polysilicon film of about 500nm in thickness.
In other words, the storage electrode is made by
depositing a polysilicon film and then merely patterning
it to the shape of the storage electrode. According to the
5 second embodiment, the storage electrode is of a structure
with the storage capacitance increased by increasing the
thickness of the polysilicon film and utilizing the
vertical components of the sidewalls of the polysilicon.
This capacitor offers the same effects as with the crown-
10 shaped capacitor in the first embodiment.

Note that the capacitor structure is the same as
that in the first embodiment excepting that the storage
electrode 26 is connected through the opening of the
silicon dioxide film 14 to the plug electrode 11 of
15 titanium nitride formed on the highly-doped n-type
impurity region 8 of the MISFET. The dielectric film 27
uses a high dielectric film, such as tantalum pentoxide
like in the first embodiment.

Fig. 12 is a sectional view of a dynamic RAM
20 different from that in Fig. 11. In Fig. 12, the storage
electrode 30 is formed by a platinum film about 100nm
thick. A capacitor dielectric film 31 made of a (Ba, Sr)
TiO$_3$) about 30nm thick is formed on the storage electrode
30. A plug electrode 29, which passes through the silicon
25 dioxide film 14, is formed in the silicon dioxide film 14
on the wiring electrode 13. Therefore, the storage
electrode 30 is connected through the plug electrode 29 to
the plug electrode 11 and further electrically connected

to the MISFET. Thus, it is possible to use an electrode material that cannot be deposited by a CVD method for better step coverage in forming the storage electrode.

In the second embodiment, as with the plug
5 electrode 11, titanium nitride is preferably used as the material for the plug electrode 29, in which case, when a storage electrode of platinum is connected to the top of the plug electrode 29, no reaction occurs between those electrodes.

10 In the second embodiment, because a capacitor dielectric film with a high dielectric constant is used, a sufficient storage capacitance can be secured even if a three-dimensional capacitor using the sidewalls of the storage electrode mentioned above is not formed.

15 Since the storage electrode is thin, the capacitor dielectric film 31 can be formed by sputtering, thus facilitating the manufacture of the dielectric film.

The capacitors described in the two embodiments are made by simpler manufacturing processes than in the
20 crown-shaped capacitor in the first embodiment.

As is obvious from the foregoing, the present invention can be applied regardless of the structure of the capacitor.

The capacitor dielectric films with a high
25 dielectric constant as mentioned above need to be annealed at a high temperature of about 750°C for crystallization. In the present invention, however, because plug electrodes of titanium nitride are used for connection to the

substrate silicon, they do not react with the silicon at the connection points.

The structure of the plug electrode 29 shown in Fig. 12 in the second embodiment can be applied to the crown-shaped capacitors in the first embodiment and to capacitors in other embodiments.

<Embodiment 3>

A third embodiment relates to the dynamic RAM in the first embodiment and more particularly to the connection method of the storage electrode. Fig. 13 is a sectional view of the dynamic RAM in the third embodiment and shows a method of reducing the diameter of the openings of the silicon dioxide film 14 when connecting the capacitor storage electrode 15 to the plug electrode 11. In Fig. 13, the structure is identical with that in Fig. 1 excepting for the openings of the silicon dioxide film 14. Plug electrodes of titanium nitride are provided on the highly-doped n-type impurity regions of the MISFETs formed on a silicon substrate, and crown-shaped capacitors are formed through the intermediary of the silicon dioxide film 14 over the data line. The openings formed in the silicon dioxide film 14 are decreased in diameter by spacer insulators 33 along the sidewalls of the openings. The capacitor storage electrodes 16 are connected to the plug electrodes 11 through the openings narrowed as described.

The manufacturing process of the third embodiment will be described with reference to Figs. 14 to 17.

As shown in Fig. 14, the process until MISFETs and data lines are formed on the silicon substrate is the same as in Fig. 7 showing the first embodiment. Subsequently, a silicon dioxide film 14 is deposited on

5 the wiring electrode 13, and openings about 0.2 μ m in diameter are formed in the silicon dioxide film 14 by photolithography and dry etching. The 0.2 μ m is the minimum processing dimension in photolithography.

After this, as shown in Fig. 16, a silicon

10 nitride film about 50nm thick is deposited by a LPCVD method, and a silicon nitride film is formed on the sidewalls of the openings with better covering properties. A spacer insulator 33 is formed on the sidewalls of the openings of the silicon dioxide film 14 by etch-back of

15 the flat portion of the deposited silicon nitride by anisotropic dry etching. After the spacer insulators 33 have been formed, the underneath silicon nitride film 12 may be etched away by overetch to form openings to the plug electrodes 11. By the above-mentioned process, the

20 openings of the silicon dioxide film 14 becomes about 0.1 μ m in diameter.

After this, as shown in Fig. 17, a polysilicon film for storage electrode is deposited, the crown-shaped storage electrodes 15 are formed as in the first

25 embodiment, and a capacitor dielectric film 16 and a plate electrode 17 are formed.

According to the third embodiment, in the silicon dioxide film 14 on the wiring electrode 13 as the

data line, the openings are formed with a diameter less than the minimum processing dimension, so that the space between the data line and the opening can be reduced and the short margin between the storage electrode and the

5 data line can be increased. According to the third embodiment, description has been made by taking the crown-shaped capacitor as an example, but this embodiment can be applied to the capacitor structure in the second embodiment and other well-known capacitor structures.

10 <Embodiment 4>

A fourth embodiment of the present invention relates to the dynamic RAM in the first embodiment and also to a method of reducing the line width of the data line. Fig. 18 is a sectional view of the dynamic RAM

15 according to the fourth embodiment.

In Fig. 18, a wiring electrode 37 as the data line is embedded at the opening formed in the silicon dioxide film 35. A spacer insulator 36 formed by a silicon nitride film is formed at this opening, and the line width

20 of the wiring electrode 37 is determined by the spacer insulator 36. Crown-shaped capacitor storage electrodes 15 are formed over the wiring electrode 37 and on the silicon dioxide film 38 on the silicon dioxide film 35. The storage electrode 15 is connected to the plug electrode 11

25 through a common opening running through the silicon dioxide films 38, 35 and the silicon nitride film 12.

The fourth embodiment will be described with reference to sectional views of the manufacturing process

shown in Figs.19 to 24.

As shown in Fig. 19, the manufacturing process until the MISFETs and the plug electrodes 11 are formed on the silicon substrate is the same as in Fig. 6 showing the first embodiment. Further, a silicon nitride film 12 is deposited to a thickness of about 50nm by a LPCVD method.

After this, as shown in Fig. 20, a silicon dioxide film 35 about 200nm in thickness is deposited by CVD using a TEOS gas, openings are formed in the silicon dioxide film 35 according to a pattern of the wiring electrode, and a silicon nitride film 41 about 50nm thick is deposited with better covering properties by a LPCVD method. Note that a silicon dioxide film may be used instead of the silicon nitride film.

Subsequently, as shown in Fig. 21, the silicon nitride films 41 and 12 are etched by anisotropic dry etching, a spacer insulators 36 are formed on the sidewalls of the silicon dioxide film 35, and at the same time the plug electrode 11 is exposed.

Next, as shown in Fig. 22, a tungsten film about 300nm thick is deposited. A CVD method is preferred as the deposition method. After this, the tungsten film on the silicon dioxide film 35 is polished by a CMP method to leave the tungsten embedded only in the openings of the silicon dioxide film 35. In this step, it is made sure that the tungsten film is polished about 50 to 100nm in excess.

Subsequently, as shown in Fig. 23, a silicon

dioxide film 38 is deposited to a thickness of 100nm, and common openings 42 are formed to run through the silicon dioxide films 38, 35 and the silicon nitride film 12. Incidentally, better effects can be achieved if the

5 openings are formed in combination with the third embodiment.

After this, as shown in Fig. 24, a polysilicon used as the storage electrodes 15 is deposited and crown-shaped capacitors are formed as in the first embodiment.

10 According to the fourth embodiment, because the line width of the wiring electrode 37 as the data line can be reduced to less than the minimum-processing dimension, the short margin between the wiring electrode 37 and the openings for connection to the storage electrodes 15 can

15 be increased.

In the fourth embodiment, description has been made by taking the crown-shaped capacitor as an example, but this embodiment can be applied to the capacitor structure described in the second embodiment and other

20 well-known capacitor structures.

This embodiment can be applied to memory cells that do not use plug electrodes on the silicon substrate as depicted in Fig. 25 and also to memory cells that use polysilicon plugs.

25 Further, the fourth embodiment can be used not only to the dynamic RAM but also to wiring used in LSI circuits. In this case, as the material for the wiring electrode 37, a low resistivity metal such as aluminum or

copper can be used in addition to high refractory metal with heat resistance.

<Embodiment 5>

A fifth embodiment of the present invention
5   relates to a memory cell of dynamic RAM type, which uses platinum for the capacitance electrode of the capacitor, and more particularly relates to micro-scale processing of a platinum electrode. Fig. 26 shows the manufacturing process of a dynamic RAM according to the fifth embodiment,
10   in which platinum is used for the capacitance electrode of the capacitor in order that a BST film of high dielectric constant or a PZT film of ferro-dielectric is used for the capacitor of a memory cell.

As shown in Fig. 26, MISFETs are formed on the
15   silicon substrate. The manufacturing process until the plug electrodes 11 and the wiring electrodes 13 are formed is the same as the process up to Fig. 7 in the first embodiment.

After this, as shown in Fig. 27, a silicon
20   dioxide film 14 about 0.5 to 1 μm is deposited at a temperature of about 400°C by a well-known CVD method using a TEOS gas, and the surface is flattened by a well-known CMP method. Further, when openings are formed in the silicon dioxide film 14 and the silicon nitride film 12 by
25   photolithography and dry etching, and a titanium nitride film about 200nm thick is deposited by a CVD method. After this, the plug electrodes 29 are formed by etch-back of the deposited titanium nitride film at the flat portion by

anisotropic dry etching.

Subsequently, as shown in Fig. 28, a platinum film 45 with a thickness of 100 to 300nm is deposited by sputtering, and an amorphous silicon film 43 is deposited
5   to a thickness of about 100nm. The amorphous silicon film 43 is patterned by photolithography and dry etching.

Next, as shown in Fig. 29, the multilayered body thus produced is annealed to let the amorphous silicon film 43 and the platinum film 30 react each other to form
10   platinum silicide 44 at the patterned portions. That portion of the platinum film 30 where there was no amorphous silicon film remains as is.

After this, as shown in Fig. 30, the platinum silicide 44 is removed by wet etching using a hydrofluoric
15   acid solution, and thus platinum electrodes 30 are formed. It is advisable to provide a stopper to wet etching beneath the platinum films 30, though this step is omitted here.

Further, as shown in Fig. 30, a BST film 30 is
20   deposited on the platinum film 30 by sputtering or CVD, and a platinum film 32 is deposited additionally, which is patterned by photolithography and dry etching. The subsequent process may be the same as in the first embodiment.

25   According to the fifth embodiment, the platinum electrodes can be patterned in a fine geometry without directly etching the platinum film. Therefore, it is possible miniaturize a capacitor which uses the platinum

film as the storage electrode.

<Embodiment 6>

A sixth embodiment of the present invention relates a static RAM to which the present invention is

5   applied. Fig. 32 shows an equivalent circuit of the memory cell of a static RAM. The memory cell comprises a flip-flop circuit having a pair of inverters, which include n-channel MISFETs (Q1, Q2) and p-channel MISFETs (Q5, Q6), arranged in cross connection, and transfer transistors (Q3,

10 Q4) connected to the flip-flop. Figs.33 and 34 are plan views each showing a static RAM of a structure suitable for high element integration, which has p-channel MISFETs formed in polysilicon layers. Fig. 33 shows the MISFET portions formed on the silicon substrate, while Fig. 34

15 shows the TFT (Thin Film Transistor) portions and the wiring electrode portions formed in the polysilicon film.

In Fig. 33, the gate electrodes of the driver MISFETs are connected to storage nodes formed by highly-doped n-type impurity regions 106, 107 as the respective

20 drains through plug electrodes 117 of titanium nitride formed in the openings. Further, plug electrodes 117 of titanium nitride in the openings of the highly-doped n-type impurity regions 108, 109 as the sources of the driver MISFETs are connected to the ground lines 116.

25 Further, the highly-doped n-type impurity regions 106, 107 at the storage nodes also serve as highly-doped impurity regions of the transfer MISFETs Q3, Q4, and the gate electrodes 110, 111 of the transfer MISFETs serve as word

lines common to adjacent memory cells. Plug electrodes 117
are formed in the openings of the highly-doped n-type
impurity regions 104, 105 of the transfer MISFETs, and the
plug electrodes 117 are connected to the wiring electrodes

5   129,130 (Fig. 34) as the data lines.

In Fig. 34, plug electrodes 117 formed in the
storage nodes are connected through openings 140, 141 to
the gate electrodes 119, 120 of the p-channel TFTs (Q6,
Q5) as the load elements. Further, the gate electrodes 119,

10   120 are connected through openings 121, 122 to the drain
regions 114, 115 of the other TFTs. The source regions 125,
126 of the TFTs (Q5, Q6) are the common power supply
wirings for the adjacent memory cells.

Referring to Fig. 35, the sixth embodiment will

15   be described in greater detail. Fig. 35 is a sectional
view taken along the line X-X' in the plan views in
Figs.33, 34.

The n-channel MISFETs of the memory cell are
formed on the surface of the silicon substrate. The plug

20   electrodes 117 are formed on the highly-doped n-type
impurity regions 104, 106 and the gate electrode 112. The
wiring electrode 116 of the structure described in the
fourth embodiment is formed on the silicon dioxide film
133. Tungsten is preferred as the material for the wiring

25   electrode 116. The wiring electrode 116 acts as the ground
line to supply a ground potential to the source of the
sources of the driver MISFETs. The gate electrodes 119,
120 of TFTs, which are made of a p-type polysilicon film,

are formed over the wiring electrode 116 through the intermediary of the silicon dioxide film 137. A gate insulator 138 for the TFT is formed on the gate electrode 120. The TFT channel region 123 made of polysilicon, a

5 source region 125 and a drain region 114 are formed on the gate electrode 138. The drain region 114 of one TFT is connected through an opening, formed at a part of the gate insulator 138, to the gate electrode 119 of the other TFT, by which the cross connection of the flip-flop can be

10 achieved. Further, this gate electrode 119 is connected to the plug electrode 117 through an opening which is smaller than the diameter of the plug electrode 117.

According to the sixth embodiment, because a large short margin can be secured between the ground line

15 of the memory cell and the gate electrodes of the TFTs, the memory cell area of the static RAM can be reduced. Further, because the p-channel TFT and the n-channel MISFET formed on the silicon substrate are connected through a plug electrode made of titanium nitride, an

20 electrically ohmic contact can be obtained.
<Embodiment 7>

A seventh embodiment of the present invention is an application of the present invention to a static RAM in which an n-channel MISFET and a p-channel MISFET are all

25 formed on a silicon substrate. Figs.36 and 37 are plan views of static RAMs according to the seventh embodiment. Fig. 36 shows MISFETs and local wiring area and Fig. 37 shows wiring electrodes.

In Fig. 36, MISFETs Q1, Q2, Q3, Q4, Q5 and Q6 correspond to the equivalent circuit in Fig. 32. A gate electrode 215 is a gate electrode for Q1 and Q5. A gate electrode 216 is a common gate electrode for Q2 and Q6.

5   Plug electrodes 217, 218, 219 and 220 are formed on the highly-doped n-type impurity regions 206, 207 of the n-channel MISFETs Q1, Q2, Q3 and Q4 and on the highly-doped p-type impurity regions 210, 211 of the p-channel MISFETs Q5, Q6. Plug electrodes 221 and 222 are formed on the gate

10   electrodes 215, 216. In other words, the cross connection of the flip-flop of the memory cell is formed by the plug electrodes 217, 218, 219, 220, 221 and 222 and local wirings 223 and 224 formed by a tungsten film of about 100nm in thickness. Those plug electrodes are made of

15   titanium nitride, are formed by a similar method as in the first embodiment and the range of their height is from 50nm to 150nm or so.

Metal wirings 231, 232, 233, 234 in the first layer shown in Fig. 37 are installed through openings 225,

20   226, 227, 228, 229 and 230 in the highly-doped n-type impurity regions 204, 205 of MISFETs Q3 and Q4, the highly-doped n-type impurity regions 208, 209 of MISFETs Q1 and Q2 and the highly-doped p-type impurity regions 212, 213 of MISFETs Q5, Q6. The metal wiring 233 is ground

25   wiring to supply ground potential to the sources of the driver MISFETs Q1 and Q2. The metal wiring 234 is power supply wiring to supply power to the sources of driver MISFETs Q1 and Q2. Further, the data lines of the memory

cell are formed by metal wirings 237, 238 of the second layer. The metal wirings 231, 232, 233, 234, 237 and 238 are made of aluminum.

Fig. 38 is a sectional view of the seventh

5 embodiment. The n-channel MISFET and the p-channel MISFET in the memory cell are formed respectively in a p-well 244 and an n-well 245 in a silicon substrate 201. In the seventh embodiment, as in the first embodiment, silicon nitride films 239, 240 are provided at the top and

10 sidewalls of the gate electrode of the MISFETs so that self-aligned contacts can be formed. In this case, when forming the plug electrodes 217 on the gate electrode 216, photolithography and dry etching, different from those processes used in forming other plug electrodes, should

15 preferably be carried out. Though not shown, if silicon nitride is used as the etching stopper for the isolation, a structure is obtained that can be borderless.

According to the seventh embodiment, the local wiring can be microminiaturized, so that a static RAM with

20 high device integration can be provided.

<Embodiment 8>

An eighth embodiment of the present invention is an improved version of the static RAM in the seventh embodiment, in which the cross connection of the flip-flop

25 circuit can be achieved with four plug electrodes. Fig. 39 is a plan view of the static RAM according to the eighth embodiment, in which the wiring electrode portion, being identical to that in the seventh embodiment, is omitted

here. Fig. 40 is a sectional view. In Figs.39 and 40, the plug electrode 217 on the highly-doped n-type impurity region 206 of the driver MISFET is connected to the local wiring 221 formed by tungsten about 100nm thick, which is

5   above the plug electrode 217. The local wiring 221 is also connected to the common gate electrode 216 of the mating inverter (Q2, Q6) and at the same time to the highly-doped p-type impurity region 210 of the load MISFET Q5, by a plug electrode 246 which extends on the common electrode

10   246 and the region 210. A plug electrode 247 in Fig. 39 is connected in a similar manner. The above-mentioned plug electrodes are made of titanium nitride, and formed by the same method as in the first embodiment.

According to the eighth embodiment, the local

15   wiring can be further miniaturized and a static RAM with high device integration can be provided.

<Embodiment 9>

A ninth embodiment of the present invention relates to a memory cell of another system in the static

20   RAM according to the present invention. Figs.41 and 42 are plan views of the memory cell of the static RAM according to the ninth embodiment. Fig. 41 shows MISFETs and Fig. 42 shows wiring electrodes. In Fig. 41, for the cross connection of the flip-flop circuit, plug electrodes 318,

25   319, 320, 321 and 322 are used for connections without using local wirings. Those plug electrodes are made of titanium nitride, and formed by the same method as in the first embodiment. The wiring electrodes are made of two

layers of aluminum as in the seventh embodiment.

According to the seventh embodiment, the manufacturing process of the static RAM can be simplified.

In the embodiments of the memory cell described

5   above, both in a static RAM and a dynamic RAM, the indirect peripheral circuit uses plug electrodes of a common self-aligned structure explained in the first embodiment, so that the required area of the indirect peripheral circuit can be reduced.

10   In the embodiments described above, the present invention is applied to those semiconductor devices in which a static RAM and a dynamic RAM coexist on the same silicon substrate or other semiconductor devices in which memory devices and logic circuits exist side-by-side.

15 Therefore, production cost can be reduced, data transfer rate can be increased, and chip area can be decreased.

As has been described, according to the present invention, it becomes possible to reduce the required area for CMISFETs not only in the memory cells but also in the

20 indirect peripheral circuits. In a memory cell of a multilayered structure in which a device is formed above a MISFET, when the memory cell undergoes a hot working process necessary for its formation, the electrical characteristics of the connections between the plug

25 electrodes and the silicon substrate are not impaired. Thus, the memory cells are provided with stable characteristics.

Further, the short margin between the element

located at a higher position and a wiring layer at a middle position of the MISFET can be increased. Therefore, it becomes possible to provide a semiconductor device with a smaller chip area.

5   According to the present invention, it is possible to provide a semiconductor memory device capable of much higher-speed operations by the use of a low resistivity metal, such as copper, for the wiring layer above the capacitor in the memory cell region and for the

10   wiring layer in the indirect peripheral circuit region.

INDUSTRIAL APPLICABILITY

In the embodiments described above, the present invention has been applied to the dynamic RAM and the

15   static RAM.

However, the present invention can be applied to semiconductor integrated circuit devices, such as an on-chip LSI in which memory and logic (logic circuits) exist commingled. In this case, a wiring layer of the logic

20   portion can be formed at a height where there is a capacitor. The logic portion comprises a plurality of CMISFETs. In other words, the logic portion is formed by COS logic.